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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,171	12/07/2001	Jean Louis Calvignac	RAL920010016US1	5856

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IBM CORPORATION
PO BOX 12195
DEPT 9CCA, BLDG 002
RESEARCH TRIANGLE PARK, NC 27709

EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,171	CALVIGNAC ET AL.	
	Examiner	Art Unit	
	Nilesh Shah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/12/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18 are presented for examination.

Specification

2. The cross reference related to the application cited in the specification must be updated (i.e. update the relevant status, with the PTO serial numbers or patent numbers where appropriate, on page 1 lines 4-7). The entire specification should be so revised.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laurenti et al (6,658,578) (hereinafter Laurenti) in view of Koga (5,530,904).

5. As per claim 1, Laurenti teaches the invention substantially as claimed including a parallel processing system comprising:

N task orientated processing devices, wherein N is greater than 1 and each of the

task-oriented devices providing a particular function (fig. 1, 10; col. 1 lines 51-65;col. 2 lines 50-57;col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46); and

M buffers, M greater than 1, each one adaptable to operate in a plurality of different phases operatively coupled to the N task orientated processing devices (col. 176 lines 20-35; col. 79 lines 15-25;col. 8 lines 39-57).

6. Laurenti does not specifically teach the use of a Time Division Multiplex controller.

   Koga teaches a Time Division Multiplex Control mechanism operatively connected to the M buffers and imposing respective ones of the different phases on said M buffers (col. 3 lines 50-57; col. 2 lines 10-23; col. 7 lines 32-50).

7. It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Laurenti and Koga because Koga's Time Division Multiplex Control mechanism would improve Laurenti's system by allowing the segments to be divided into time segments thus making the system more efficient.

8. As per claim 2, Laurenti teaches the parallel processing system wherein M = N (col. 1 lines 51-65;col. 2 lines 50-57;col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46).

9. As per claim 3, Laurenti teaches the parallel processing system wherein the particular function includes cryptography (col. 75 lines 15-40; col. 111 lines 28-33;col. 304 lines 3-10).

10. As per claim 4, Laurenti teaches the parallel processing system further including an input bus operatively coupled to the M buffers (col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46);
an output multiplexer operatively coupled to outputs of the M buffers and an output bus coupled to the output multiplexer (col. 47 lines 8-15; table 45; col. 159 lines 45-62).

11. As per claim 5, Laurenti teaches the parallel processing system wherein the plurality of different phases include a Fast Write Phase, a Slow Read Phase, a Slow Write Phase and a Fast Read Phase (fig. 15, 16,19,20,23,24,140; col. 157 lines 50-60; col. 158 lines 1-28; col. 166 lines 37-48; col. 154 lines 60-65; col. 161 lines 1-12).

12. As per claim 6, Laurenti teaches the parallel processing system wherein said each one of the M buffers further includes a slow write port receiving data if said each one of the M buffers is in the Slow Write Phase, a slow read port providing data if said each one of the M buffers is in the Slow Read Phase, a fast write port receiving data if said each one of the M buffers is in a Fast Write Phase and a Fast Read Phase providing data if said each one of the M buffers is in a Fast Read Phase (fig. 15, 16,19,20,23,24,140; col. 157 lines 50-60; col. 158 lines 1-28; col. 166 lines 37-48; col. 154 lines 60-65; col. 161 lines 1-12).

13. As per claim 7, Laurenti teaches wherein the mechanism includes one slow read address generator operatively coupled to at least one of the M buffers, one Slow Write address generator (fig. 38; col. 9 lines 5-31) operatively coupled to the at least one of the M buffers, one Fast Read address generator operatively coupled to the at least one of the M buffers, and at least one fast right address generator operatively coupled to said at least one of the M buffers (col. 157 lines 50-60; col. 158 lines 1-28; col. 166 lines 37-48; col. 154 lines 60-65; col. 161 lines 1-12) and Read Reset signal that drives the slow read address generator and the at least one Fast read address generator and a write reset signal that drives the fast write address generator and the slow write address generator (fig. 15, 16,19,20,23,24,140; col. 157 lines 50-60; col. 158 lines 1-28; col. 166 lines 37-48; col. 154 lines 60-65; col. 161 lines 1-12).

Koga teaches a Time Division Multiplex Control mechanism (col. 3 lines 50-57; col. 2 lines 10-23; col. 7 lines 32-50).

14. As per claim 8, Laurenti teaches the parallel processing system wherein the address generator includes a binary counter (col. 178 lines 52-67; col. 9 lines 5-31);

an address bus operatively coupled to the binary counter(col. 178 lines 52-67);

a decoder operatively coupled to the address bus and an inverter operatively coupled to the decoder(col. 75 lines 15-40; col. 111 lines 28-33;col. 304 lines 3-10);

an OR gate having a first input coupled to the inverter and a second input coupled to a Reset signal (col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37);

an AND gate having a first input coupled to the OR gate, a second input coupled to a clock line and an output coupled to the binary counter(col. 75 lines 15-40; col. 111 lines 28-33;col. 304 lines 3-10).

Koga teaches a Time Division Multiplex Control mechanism (col. 3 lines 50-57; col. 2 lines 10-23; col. 7 lines 32-50).

15. As per claim 9, Laurenti teaches the parallel processing system wherein the control circuit arrangement includes a time base free naming counter (col. 178 lines 52-67; col. 9 lines 5-31);

a Reset Decoder operatively coupled to the output of the time base, free naming counter (col. 176 lines 20-32; col. 132 lines 36-67);

a circuit arrangement that monitors space available in each of the M buffers and outputs a control pulse if the available space is less than the space required to store a predetermined size data block (col. 1 lines 51-65;col. 2 lines 50-57;col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46);

a delay line; and a buffer counter operatively coupled to the delay line and the circuit arrangement (fig 61, 68, 93; col. 110 lines 50-67).

Koga teaches a Time Division Multiplex Control mechanism (col. 3 lines 50-57; col. 2 lines 10-23; col. 7 lines 32-50).

16. As per claim 10, Laurenti teaches the parallel processing system wherein

providing at least one process engine that provides a predetermined task,

providing at least one buffer operatively coupled to the process engine (col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46);

putting the at least one buffer in a fast write mode wherein data is received and written into said buffer at a first speed (table 95; col.165 lines 12-25; col. 149 lines 65-15);

putting the buffer in a slow read mode wherein data is read from the buffer into the at least one process engine at a second speed (col. 2 lines 50-57;col. 98 lines 1-45; col. 98 lines 55-67; col.165 lines 12-25; col. 149 lines 65-15);

activating the at least one process engine to process data read out of the buffer(col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46);

putting the at least one buffer in slow write mode wherein processed data is written into the buffer from the at least one process engine at a third speed(table 95; col.165 lines 12-25; col. 149 lines 65-15; and

putting the at least one buffer in a fast write mode wherein processed data is read out of the buffer at the same speed and sequence as the speed and sequence at which the data was received (col.165 lines 12-25; col. 149 lines 65-15; col. 166 lines 37-48; col. 154 lines 60-65; col. 161 lines 1-12).

Koga teaches a Time Division Multiplex Control mechanism (col. 3 lines 50-57; col. 2 lines 10-23; col. 7 lines 32-50).

17. As per claim 11, Laurenti teaches the parallel processing system wherein the particular function includes cryptography (col. 75 lines 15-40; col. 111 lines 28-33;col. 304 lines 3-10).

18. As per claim 12, Laurenti teaches a system wherein:

at least one buffer having a first connection that ports to a network, a second connection that ports to a network, a third connection that ports to a process and a fourth connection that ports to the process (abstract; col. 8 lines 37-49; col. 8 lines 60-67) ; and

a control circuit that generates a Fast Write Phase in which data is received at the first connection at a first speed, a Slow Read Phase at which data is transferred from the buffer through the third connection at a second speed, a Slow Write Phase in which data

is written from the fourth connection into the buffer at the second speed and a Fast Read

Phase in which data is transferred from the buffer to the second connection at the first speed (fig. 15, 16,19,20,23,24,140; col. 157 lines 50-60; col. 158 lines 1-28; col. 166 lines 37-48; col. 154 lines 60-65; col. 161 lines 1-12).

Koga teaches a Time Division Multiplex Control mechanism (col. 3 lines 50-57; col. 2 lines 10-23; col. 7 lines 32-50).

19. As per claim 13, Laurenti teaches a system further including a process engine operatively coupled to the third connection and the fourth connection (abstract; col. 8 lines 37-49; col. 8 lines 60-67).

20. As per claim 14, Laurenti teaches a system wherein: the process engine includes a cryptographic unit (col. 75 lines 15-40; col. 111 lines 28-33;col. 304 lines 3-10).

21. As per claim 15, Laurenti teaches a parallel processing system wherein the predetermined size data block includes a data frame or data packet. (col. 158 lines 1-28; col. 166 lines 37-48; col. 154 lines 60-65; col. 161 lines 1-12).

22. As per claim 16, Laurenti teaches a parallel processing system wherein the space monitoring circuit arrangement includes a boundary MUX having an input from the buffer counter and a plurality of inputs of boundary signals one from each buffer indicating address reached in each buffer at end of fast write phase(col. 9 lines 21-30; col. 2 lines 50-57;col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46);

a subtractor responsive to output signal from the boundary MUX and output signal from the time base counter(col. 9 lines 21-30; col.165 lines 12-25; col. 149 lines 65-15; col. 166 lines 37-48); and

a comparator responsive to an output signal from said subtractor and a signal indicating length of the data frame (col. 9 lines 21-30).

23. As per claim 17, Laurenti teaches a parallel processing system wherein the particular function includes any data processing system (fig. 1, 10; col. 1 lines 51-65;col. 2 lines 50-57;col. 98 lines 1-45)

24. As per claim 18, Laurenti teaches a parallel processing system wherein the particular function includes any data processing function whose processing time is proportional to frame length (col. 98 lines 1-45; col. 98 lines 55-67; col. 99 lines 24-37; col. 100 lines 10-46).

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2195

NS
May 23, 2005

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100